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Description

[METHOD FOR FORMING NITRIDED TUNNEL OXIDE LAYE]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention relates to a semiconductor process. More particularly, the present invention relates to a method for forming a nitrided tunnel oxide layer of non-volatile memory.

[0003] Description of the Related Art

[0004] Accompany with the continuous reduction of the price per unit memory size, electrically erasable programmable read-only memory (EEPROM) devices are more often used as non-volatile storage devices. One essential part of an EEPROM cell is the tunnel oxide layer, which should be sufficiently thin so that carriers can tunnel through under a high electric field. The quality and stability of the tunnel oxide layer are also important issues, since the charge re-

tention capability and other important characteristics of an EEPROM device is closely related to these properties.

[0005] There have been many methods provided for improving the quality and stability of a tunnel oxide, wherein most of these methods utilize nitrogen doping in silicon oxide. For example, U.S. 5,885,870 patent and US 6,380,033 patent disclose a method for forming a nitrided tunnel oxide layer, wherein NO or N_2O-annealing is performed to nitridate a tunnel oxide layer. With the NO or N_2O-annealing treatment, the leakage current induced by negative Fowler-Nordheim stress (negative FN-SILC) and the threshold voltage (V_t) shift of an EEPROM device can be reduced. However, the method cannot effectively reduce the leakage current induced by a positive FN stress (positive FN-SILC), and the distribution window of the incorporated nitrogen atoms is small in accordance to this method. Moreover, nitrogen atoms tend to pile up at the bottom interface of the tunnel oxide layer according to this method, so that the carrier mobility and the integrity of the periphery gate oxide of the EEPROM device are degraded.

[0006] In addition, the US 6,559,007 patent discloses another method for forming a nitrided tunnel oxide layer, wherein

NH_3-anealing is performed to nitridate a tunnel oxide layer for inhibiting diffusion of hydroxyl and hydrogen species in the tunnel oxide layer. However, the integrated process in this method is quite complicated, and the distribution window of the incorporated nitrogen atoms is small as in the case of NO or N_2O-annealing. Similarly, nitrogen atoms also tend to pile up at the bottom interface of the tunnel oxide layer according to this method. Meanwhile that the carrier mobility and the integrity of the periphery gate oxide of the EEPROM device are degraded.

[0007] On the other hand, the US 6,551,948 patent discloses a method for forming an oxynitride film in inter-poly dielectric applications, wherein a polysilicon film is exposed to plasma formed by exciting a mixed gas containing oxygen and nitrogen. In addition, the US 6,413,881 and US 6,548,366 patents disclose methods for forming an ultra-thin gate oxide layer, wherein nitrogen plasma is used to nitridate an ultra-thin gate oxide layer for inhibiting impurity diffusion.

SUMMARY OF INVENTION

[0008] Accordingly, this invention provides a method for forming a nitrided tunnel oxide layer. The method is capable of reducing positive or negative FN-SILC and V_t shift without

the problems of lower carrier mobility and degraded periphery gate oxide integrity caused by the NO or N_2O-annealing method as in the prior art.

[0009] The method for forming a nitrided tunnel oxide layer of this invention includes the following steps. A silicon oxide layer as a tunnel oxide layer is formed on a semiconductor substrate, and a plasma nitridation process is performed to implant nitrogen atoms into the silicon oxide layer. Then, a thermal drive-in process is performed to diffuse the implanted nitrogen atoms across the silicon oxide layer.

[0010] By using the method of this invention to form a nitrided tunnel oxide layer, the low-field SILC and V_t shift of the memory device can be reduced. Moreover, with the nitridation method of this invention, the incorporated nitrogen atoms will not pile up at the bottom interface of the silicon oxide layer. Therefore, degradation of the carrier mobility or the integrity of the periphery gate oxide of the memory device can be prevented.

[0011] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0012] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0013] FIGs. 1A-1C illustrate a process flow of forming a nitrided tunnel oxide layer according to a preferred embodiment of this invention.

[0014] FIG. 2 shows the results of a negative FN-SILC test on different memory samples, wherein the memory sample of this invention is labeled with "ISSG 85Åoxide + Plasma nitridation + Thermal drive-in".

[0015] FIG. 3 shows the results of a positive FN-SILC test on the above memory samples.

[0016] FIG. 4 shows the results of a V_t-shift test on the above memory samples.

[0017] FIG. 5 shows the results of a carrier mobility test on the above memory samples.

Detailed Description

[0018] FIGs. 1A-1C illustrate a process flow of forming a nitrided

tunnel oxide layer according to the preferred embodiment of this invention.

[0019] Referring to FIG. 1A, a silicon substrate 100, such as a P-doped single-crystal silicon substrate, is provided. A silicon oxide layer 110 as a tunnel oxide layer is then formed on the silicon substrate 100 with, for example, an in-situ steam generation (ISSG) process.

[0020] Referring to FIG. 1B, a plasma nitridation process is performed by exposing the silicon oxide layer 110 to nitrogen-containing plasma 120, whereby nitrogen atoms are implanted into the surface layer of the silicon oxide layer 110. The nitrogen-containing plasma 120 may be N_2 plasma, and the plasma nitridation process can be performed under a temperature lower than 400°C.

[0021] Referring to FIG. 1C, a thermal drive-in process is performed to diffuse the incorporated nitrogen atoms 130 across the silicon oxide layer 110. The thermal drive-in process can be a furnace annealing process or a rapid thermal annealing (RTA) process, and is preferably conducted under 850 to 1100°C for 30 seconds to 1 hour.

[0022] *<Examples>* In the examples, a pure ISSG oxide layer of 85Å, an ISSG oxide layer of 85Ånitrided with NO or N_2O-annealing and an ISSG oxide layer of 85Å that has been

subjected to the plasma nitridation step and the thermal drive-in step of this invention are provided respectively. Different memory samples are then fabricated based on the respective tunnel oxide layers. The quality and characteristics of each kind of tunnel oxide layer are evaluated via several tests on the above memory samples, and the results are shown in FIGs. 2-5, wherein the memory sample of this invention is labeled with "ISSG 85Å oxide + Plasma nitridation + Thermal drive-in".

[0023] Referring to FIG. 2, FIG. 2 shows the results of a negative FN-SILC test on the above memory samples. In the test, a negative FN stress about -11.5MV/cm is applied across the tunnel oxide layer of each sample for 100 seconds, and then the differential SILC (ΔSILC) of each sample is measured under a low field of 6MV/cm. As shown in FIG. 2, the capability for reducing negative FN-SILC of the method of this invention is approximately the same as that of the NO or N_2O-annealing method in the prior art.

[0024] FIG. 3 shows the results of a positive FN-SILC test on the above memory samples. In the test, a positive FN stress about 16MV/cm is applied across the tunnel oxide layer of each sample for 100 seconds, and then the differential SILC (ΔSILC) of each sample is measured under a low field

of -6MV/cm. As shown in FIG. 3, in accordance to the present invention, the capability for lowering the positive FN-SILC is even better than that of the NO or N_2O-annealing method in the prior art.

[0025] FIG. 4 shows the results of a V_t-shift test on the above memory samples. In the test, each sample is subjected to a baking treatment under 250°C for 24 hours, and then the V_t-shift (ΔV_t) distribution of each sample is measured. As shown in claim 4, at the high-ΔV_t region, the ΔV_t distribution probability of the memory sample of this invention is lower than those of the memory samples of the prior art.

[0026] FIG. 5 shows the results of a carrier mobility test on the above memory samples, wherein the carrier mobility is indicated by the magnitude of the channel current (mA). As shown in FIG. 5, the carrier mobility degradation resulted from the nitridation method is much less in this invention than that resulted from the NO or N_2O-annealing method in the prior art.

[0027] As mentioned above, by using the method of this invention to nitridate the tunnel oxide layer, the low-field SILC and V_t shift of the memory device can be reduced. Moreover, with the nitridation method of this invention, the in-

corporated nitrogen atoms will not pile up at the bottom interface of the silicon oxide layer. Therefore, degradations of the carrier mobility and the integrity of the periphery gate oxide of the memory device can be prevented.

[0028] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.